16.3 A 2.6mW 6b 2.2GS/s 4-times Interleaved Fully Dynamic Pipelined ADC in 40nm Digital CMOS

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Communication in the unlicensed frequency band around 60GHz requires a very fast ADC with low resolution. We present a four-way interleaved converter, of which one channel is shown in Fig. 16.3.1, for these requirements. Dynamic pipelined conversion enables low power quantization at high speed with low input capacitance but requires calibration. A folding front-end halves the required calibration effort.

Figure 16.3.1 shows a simplified schematic of the folding front-end and its waveforms. It samples and rectifies the input signal while removing its common-mode. When the S_1 switches are closed the input voltages are tracked across C_s. At a falling ϕ_1 edge the charges on C_s are fixed. Their bottom plates are at ground and the top plates at their sampled input voltage, neglecting charge injection. Closing S_2 shorts the top plates and generates the differential voltage at the bottom plates with some loss due to stray capacitance. The folding stage comparator is then activated, and based on its decision closes one set of switches in the chopper (at t_1), sharing the charge on the bottom plates with the next stage such that the differential output voltage is always positive. The common-mode output is independent of the common-mode input which fixes the common-mode voltage for the ADC back-end and significantly improves the common-mode input range. Moreover, the applied common-mode voltage may differ in calibration and normal operation.

Common-mode charge is added to the C_s bottom plates to ensure that the bottom plate voltages do not go below the ground potential (not shown in Fig. 16.3.1). The value of the sampling capacitance is 40 fF to limit the influence of parasitics. The 4X interleaved sampling instants are determined by passing one of every four edges of a single 2.2GHz clock buffer to the sampling switch gates using transmission gates. By design the timing skew spread due to mismatch has been limited to 0.7ps, so no timing calibration is required.

In [2] an efficient six bit comparator-based asynchronous binary search (CABS) ADC is realized that has 63 dynamic comparators with different thresholds but clocks only six of them. The conversion speed is limited as 6 comparisons occur in the same clock phase. In the proposed design, pipelining is used to increase the speed but of course amplifiers are required. Linearity requirements in these amplifiers are avoided by activating a different dynamic comparator for each ADC threshold and calibrating the corresponding comparator threshold to a desired input-referred value, cancelling errors both from non-linear signal processing and offsets in the comparators. As in [2], only a subset of the comparator tree is activated, based on the decisions of previous pipeline stages.

A block diagram of the pipelined binary search (PLBS) converter is shown in Fig. 16.3.2, with grayed-out units inactive for an example conversion. Instead of a residue, the input minus a value determined by the previous stage decision is amplified, as in [3]. Consequently, each stage output contains no information about the digital decision of that stage. Instead, the digital decision determines which of two units of the next stage is activated. In the example of Fig. 16.3.2, the first stage comparator output is positive, so the top unit of the second stage is activated. Due to a negative second stage decision the second third stage unit is activated and generates the input for a pair of two bit flash converters while stage one is reset. Because of a positive third stage decision the third of eight two-bit flash sub-converters is activated while stage two is reset.

A block diagram of the dynamic amplifiers and comparators is shown at the top of Fig. 16.3.3, circuit schematics are shown at the bottom. The dynamic amplifier uses internal comparator nodes D+ and D- to generate its differential output (through P1) while the comparator input voltages are used for common-mode feed-forward (through P2). The comparator is a modified version of [1] calibrated using digitally controllable capacitors [4] instead of a shunt input pair. The common-mode feed-forward (P2) is ignored for now. When the clock is high the circuit is reset: nodes D+, D-, aOut+ and aOut- are pulled to ground and there is no static current. At a falling clock edge D+ and D- charge up to V_{DD} with a speed depending on the input voltage. Transistors P1 briefly carry current until the voltages on D+ and D- are high enough to turn them off. At this moment, the voltages on aOut+ and aOut- are fixed and correspond to the amount of charge put in C_a by P1. This charge depends on the slope of D+ or D- and hence the input voltage, resulting in a monotonic (but not linear) input-output characteristic. The voltage gain depends on the slew rates of D+, D-, aOut+ and aOut-, and hence on the values of C_d and C_a and the drive currents of the input pair and P1 transistors. By digitally changing the values of C_d and C_a, the gain and offset of the amplifier are tuned. The circuit thus implements an extremely low-power amplifier that consumes no static current. The amplifier settling time corresponds to the time it takes for nodes D+ and D- to turn off P1, roughly 250ps in simulation, which is less than the required comparator regeneration time. The amplifier nonlinearity is compensated by the individual threshold calibration in the architecture.

Higher common-mode input decreases the slew rate of the D+ and D-, resulting in more charge put into capacitors C_a, and hence higher common-mode output level. Transistors P2 decrease the common-mode gain of the dynamic amplifier by decreasing the drive current of P1 when the common-mode input level increases.

The ADC prototype has been manufactured in a 1P7M 40nm low power CMOS process with a core chip area of 0.03 mm^2 (Fig. 16.3.7). The start-up calibration procedure runs sequentially from the first stage to the last and applies the desired ADC thresholds (with e.g. a low-speed DAC). For each stage, first the comparator threshold is calibrated using C_d. Next, the capacitors C_a are used to set the amplifier output close to the comparator thresholds of the next stage when their corresponding ADC thresholds are applied. Calibration of an ADC channel comprises 288 steps, each of which requires 1736 samples [5]. Calibration of the four channels therefore requires 2 million samples, consuming 2.3µJ ADC energy.

The calibrated INL/DNL for each channel is below 0.8LSB for a 10mV LSB (Fig. 16.3.4). Figure 16.3.5 (top) shows SNDR and SFDR vs. input frequency at 2.2GS/s, the low-frequency SNDR is 31.6 dB, limited by thermal noise, and the ERBW is 2 GHz. Figure 16.3.5 (bottom) shows the spectrum with a 1.1GHz input at 2.2GS/s. Unless a new calibration is done, 50mV change of the supply voltage degrades the low frequency SNDR by 3dB. The common-mode input must be low enough for sufficient sampling switch overdrive: less than 0.4dB SNDR degradation is seen up to 400mV common-mode inputs. Due to an unintended parasitic coupling in two of the four channels, a history correction of one LSB is done in post-processing.

The SNDR and SFDR for different clock frequencies with a near-Nyquist input are shown in the top plot of Fig. 16.3.6. The SNDR starts dropping around 2.2GS/s, to 26.2dB at 3.5GS/s. Since power consumption from the 1.1V supply is purely dynamic, the energy per conversion step is 40fJ up to 2.2GS/s (bottom plot of Fig. 16.3.6).

Acknowledgments:
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References:
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[5] P. Nuzzo, et al., "Efficient calibration through statistical behavioral modeling of a high-speed low-power ADC", *Proc. of PRIME*, pp. 297-300, Jun. 2006.

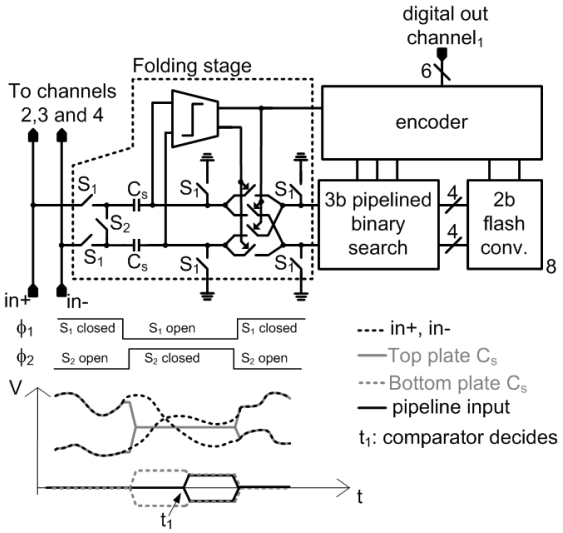

Figure 16.3.1: Architecture of one channel of the interleaved ADC (top) and waveforms in the folding stage (bottom).

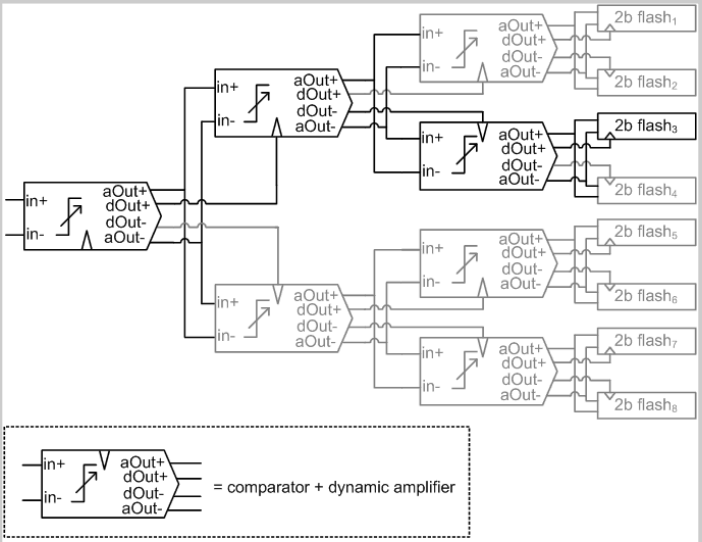

Figure 16.3.2: Architecture of the pipelined binary search conversion, grayed out parts inactive for an example conversion.

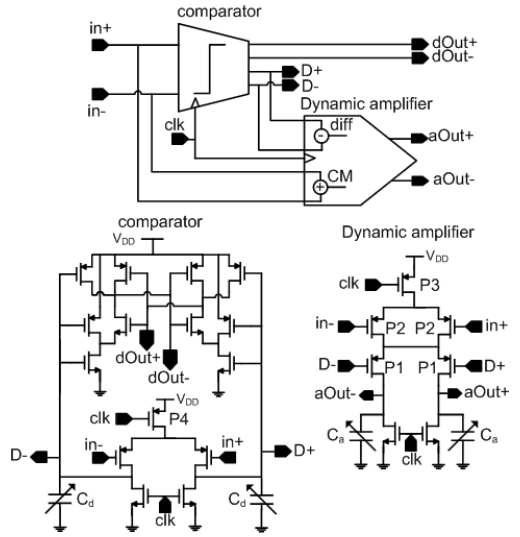

Figure 16.3.3: Block diagram and schematics of the comparator and dynamic amplifier used in the pipeline converter.

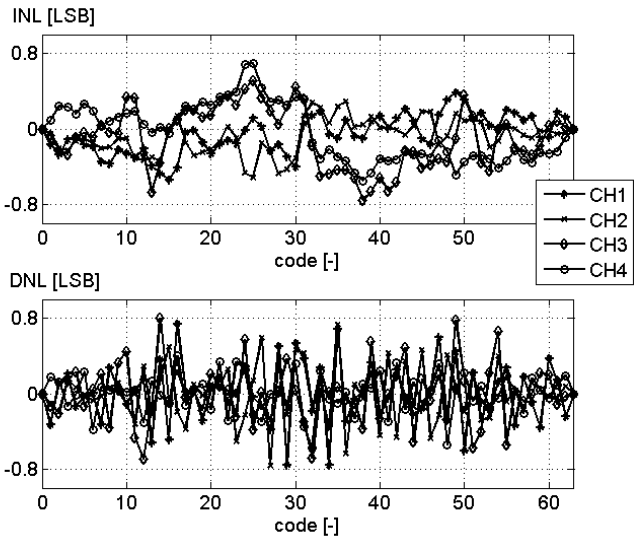

Figure 16.3.4: Calibrated INL and DNL of each ADC channel.

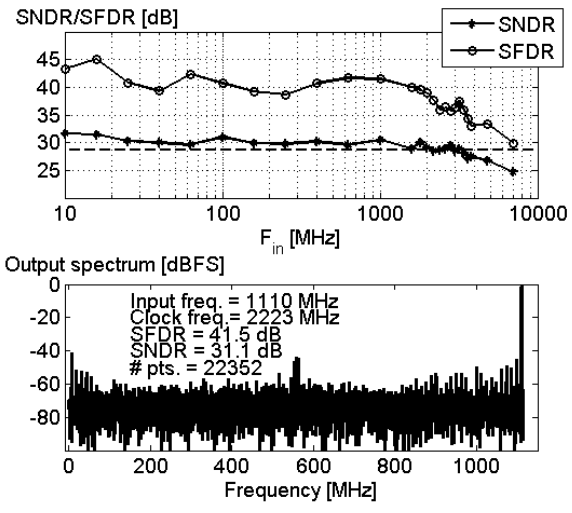

Figure 16.3.5: Measured SNDR and SFDR vs. input frequency at 2.2GS/s sampling frequency (top) and output spectrum (bottom).

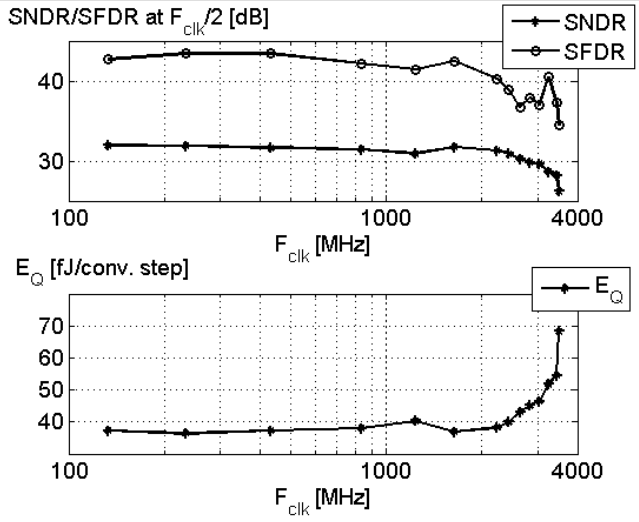

Figure 16.3.6: Measured SNDR and SFDR near Nyquist input frequency (top) and energy per conversion step (bottom) vs. clock frequency.

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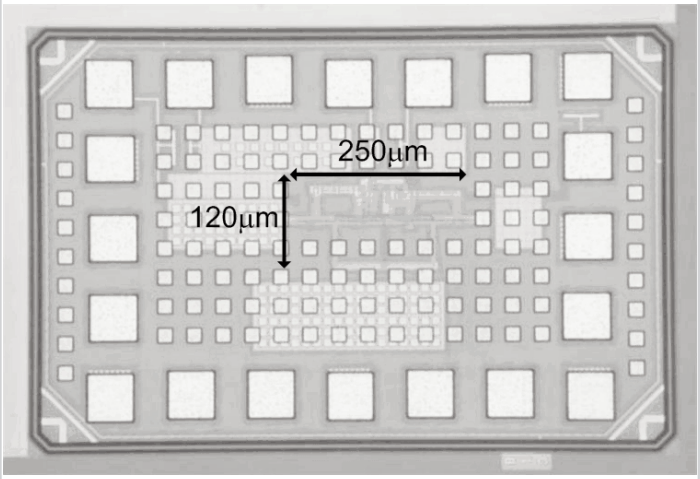

Figure 16.3.7: Chip micrograph with core size indicated.

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